Access DB# 102296

# SEARCH REQUEST FORM

**Scientific and Technical Inf rmation Center**

Requester's Full Name: Alan Diamond Examiner #: 70817 Date: 8/26/03
Art Unit: 1753 Phone Number 308-0840 Serial Number: 10/038,681
Mail Box and Bldg/Room Location: CP3, 7-B32 Results Format Preferred (circle): PAPER DISK E-MAIL

**If more than one search is submitted, please prioritize searches in order of need.**

**********

Please provide a detailed statement of the search topic, and describe as specifically as possible the subject matter to be searched. Include the elected species or structures, keywords, synonyms, acronyms, and registry numbers, and combine with the concept or utility of the invention. Define any terms that may have a special meaning. Give examples or relevant citations, authors, etc, if known. Please attach a copy of the cover sheet, pertinent claims, and abstract.

Title of Invention: Solar cell, interconnector for solar cell, and solar cell module

Inventors (please provide full names): Setoshi Tanaka

Earliest Priority Filing Date: _____

**For Sequence Searches Only* Please include all pertinent information (parent, child, divisional, or issued patent numbers) along with the appropriate serial number.*

(photovoltaic cell; solar module, solar panel, photocell; solar battery)

A solar cell that has an electrode, connector or interconnector coated with lead-free solder.

Examples of the lead-free solder are:

Sn-Bi-Ag

Sn-Ag

If there are any electrical devices that use an interconnector with lead-free solder, this would be helpful.

**********

| STAFF USE ONLY | Type of Search | Vendors and cost where applicable |
|---|---|---|
| Searcher: EIC | NA Sequence (#) | STN $65.88 |
| Searcher Phone #: | AA Sequence (#) | Dialog $82.99 |
| Searcher Location: | Structure (#) | Questel/Orbit |
| Date Searcher Picked Up: | Bibliographic ✓ | Dr.Link |
| Date Completed: 8-26-03 | Litigation | Lexis/Nexis |
| Searcher Prep & Review Time: 5 | Fulltext | Sequence Systems |
| ~~Clerical Prep Time:~~ | Patent Family | WWW/Internet |
| Online Time: 60 | Other | Other (specify) |

PTO-1590 (8-01)

STN

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=> file reg
FILE 'REGISTRY' ENTERED AT 13:31:14 ON 26 AUG 2003
USE IS SUBJECT TO THE TERMS OF YOUR STN CUSTOMER AGREEMENT.
PLEASE SEE "HELP USAGETERMS" FOR DETAILS.
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=> d his

     FILE 'REGISTRY' ENTERED AT 13:17:32 ON 26 AUG 2003
L1          9130 S (SN(L)AG)/ELS
L2           359 S L1 (L) 2/ELC.SUB
L3          1738 S L1 (L) BI/ELS
L4           287 S L3 (L) 3/ELC.SUB

     FILE 'HCA' ENTERED AT 13:22:26 ON 26 AUG 2003
L5           717 S INTERCONNECT!R?
L6          1388 S (LEADFREE? OR (LEAD OR PB)(A)(FREE# OR FREEING# OR ABSE
L7          1698 S L2
L8           266 S L4
L9             1 S L5 AND L6
L10            1 S L5 AND (L7 OR L8)
L11        39051 S INTERCONNECT?
L12           98 S L11 AND L6
L13           87 S L11 AND (L7 OR L8)
L14        45360 S SOLARCELL? OR (SOLAR? OR PHOTOELEC?)(2A)(CELL OR CELLS)
L15            1 S L12 AND L14
L16            3 S L13 AND L14

     FILE 'REGISTRY' ENTERED AT 13:27:52 ON 26 AUG 2003
L17         7839 S L1 NOT PB/ELS
L18         7734 S L17 NOT C/ELS
L19         7471 S L18 AND AYS/CI

     FILE 'HCA' ENTERED AT 13:28:40 ON 26 AUG 2003
L20         4878 S L19
L21            1 S L20 AND L5
L22          128 S L11 AND L20
L23            3 S L22 AND L14
L24            3 S L9 OR L10 OR L15 OR L16 OR L21 OR L23

     FILE 'REGISTRY' ENTERED AT 13:31:14 ON 26 AUG 2003


=> file hca
FILE 'HCA' ENTERED AT 13:28:40 ON 26 AUG 2003
USE IS SUBJECT TO THE TERMS OF YOUR STN CUSTOMER AGREEMENT.
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L24  ANSWER 1 OF 3  HCA  COPYRIGHT 2003 ACS on STN
ACCESSION NUMBER:        137:127590  HCA
TITLE:                     ***Solar***     ***cell***  , and
                         ***interconnector***  and string for
                         ***solar***     ***cell***
INVENTOR(S):             Tanaka, Satoshi
PATENT ASSIGNEE(S):      Sharp Corp., Japan
SOURCE:                  Jpn. Kokai Tokkyo Koho, 8 pp.
                         CODEN: JKXXAF
```

DOCUMENT TYPE: Patent
LANGUAGE: Japanese
FAMILY ACC. NUM. COUNT: 1
PATENT INFORMATION:

| PATENT NO. | KIND | DATE | APPLICATION NO. | DATE |
|---|---|---|---|---|
| JP 2002217434 | A2 | 20020802 | JP 2001-11603 | 20010119 |
| US 2002148499 | A1 | 20021017 | US 2002-38681 | 20020108 |

PRIORITY APPLN. INFO.: JP 2001-11603 A 20010119

AB The ***solar*** ***cell*** has electrodes coated with a ***Pb*** - ***free*** ***solder*** . The solder is also used for the ***solar*** ***cell*** ***interconnector*** and string for the ***interconnector*** .

IT ***11144-61-9*** ***157421-78-8***
( ***lead*** ***free*** ***solders*** for electrode coating and ***interconnectors*** for ***solar*** ***cells*** )

RN 11144-61-9 HCA
CN Silver alloy, nonbase, Ag,Sn (9CI) (CA INDEX NAME)

| Component | Component Registry Number |
|---|---|
| Ag | 7440-22-4 |
| Sn | 7440-31-5 |

RN 157421-78-8 HCA
CN Silver alloy, nonbase, Ag,Bi,Sn (9CI) (CA INDEX NAME)

| Component | Component Registry Number |
|---|---|
| Ag | 7440-22-4 |
| Bi | 7440-69-9 |
| Sn | 7440-31-5 |

IC ICM H01L031-04
ICS B23K001-00; B23K001-20; B23K035-26
CC 52-2 (Electrochemical, Radiational, and Thermal Energy Technology)
ST ***solar*** ***cell*** electrode ***interconnector*** ***lead*** ***free*** ***solder*** string
IT ***Solders***
( ***lead*** ***free*** ***solders*** for electrode coating and ***interconnectors*** for ***solar*** ***cells*** )
IT ***Solar*** ***cells***
( ***lead*** ***free*** ***solders*** for ***solar*** ***cell*** electrode coatings and ***interconnectors*** )
IT 7429-90-5, Aluminum, uses 7440-22-4, Silver, uses
(electrodes with ***lead*** ***free*** ***solder*** coatings for ***solar*** ***cells*** )
IT ***11144-61-9*** ***157421-78-8***
( ***lead*** ***free*** ***solders*** for electrode coating and ***interconnectors*** for ***solar*** ***cells*** )

L24 ANSWER 2 OF 3 HCA COPYRIGHT 2003 ACS on STN
ACCESSION NUMBER: 119:76313 HCA

TITLE: Method for forming ***solar*** ***cell*** contacts and ***interconnecting*** ***solar*** ***cells***
INVENTOR(S): Borenstein, Jeffrey T.; Gonsiorawski, Ronald C.
PATENT ASSIGNEE(S): Mobil Solar Energy Corp., USA
SOURCE: PCT Int. Appl., 51 pp.
CODEN: PIXXD2

DOCUMENT TYPE: Patent
LANGUAGE: English
FAMILY ACC. NUM. COUNT: 1
PATENT INFORMATION:

| PATENT NO. | KIND | DATE | APPLICATION NO. | DATE |
|---|---|---|---|---|
| WO 9222929 | A1 | 19921223 | WO 1992-US3592 | 19920430 |
| W: AU, CA, JP, KR | | | | |
| RW: AT, BE, CH, DE, DK, ES, FR, GB, GR, IT, LU, MC, NL, SE | | | | |
| US 5178685 | A | 19930112 | US 1991-713687 | 19910611 |
| AU 9219229 | A1 | 19930112 | AU 1992-19229 | 19920430 |
| AU 647285 | B2 | 19940317 | | |
| EP 542959 | A1 | 19930526 | EP 1992-911329 | 19920430 |
| R: BE, CH, DE, ES, FR, GB, IT, LI, NL | | | | |
| JP 06500670 | T2 | 19940120 | JP 1992-511474 | 19920430 |

PRIORITY APPLN. INFO.: US 1991-713687 19910611
WO 1992-US3592 19920430

AB The Ag-rich contacts are formed by firing an ink or paste contg. spherical Ag particles before firing. ***Interconnections*** between the cells are prepd. by using a Sn-(2-4)% Ag solder paste. The contacts show little or no decrease of peel strength after exposed high temps., e.g., 150.degree..

IT ***139658-38-1***
(solder, for ***interconnecting*** ***solar*** ***cells*** with silver-rich contacts)
RN 139658-38-1 HCA
CN Tin alloy, base, Sn 96-98,Ag 2-4 (9CI) (CA INDEX NAME)

| Component | Component Percent | Component Registry Number |
|---|---|---|
| Sn | 96 - 98 | 7440-31-5 |
| Ag | 2 - 4 | 7440-22-4 |

IC ICM H01L031-05
ICS H01L031-18
CC 52-2 (Electrochemical, Radiational, and Thermal Energy Technology)
ST ***solar*** ***cell*** silver elec contact
IT Electrodes
( ***photoelec*** ..- ***cell*** , silver-rich, manuf. of thermal damage-resistant)
IT 7440-22-4, Silver, uses
(elec. contacts, for ***solar*** ***cells*** , manuf. of)
IT 147625-78-3, 4942D
(in manuf. of silver-rich contacts for ***solar*** ***cells*** )
IT ***139658-38-1***
(solder, for ***interconnecting*** ***solar*** ***cells*** with silver-rich contacts)

L24 ANSWER 3 OF 3 HCA COPYRIGHT 2003 ACS on STN
ACCESSION NUMBER: 102:9622 HCA

TITLE: Alternative methods for bonding solar array ***interconnects***

AUTHOR(S): Kelly, George J.
CORPORATE SOURCE: Solarex Aerosp., Gaithersburg, MD, 20877, USA

SOURCE: Proceedings of the Intersociety Energy Conversion Engineering Conference (1984), 19th(Vol. 1), 512-17
CODEN: PIECDE; ISSN: 0146-955X
DOCUMENT TYPE: Journal
LANGUAGE: English

AB Solders and application techniques were evaluated to improve the survivability of solar-array ***interconnections*** during thermal cycling. The performance of each method was compared by visual examn. of the bonded joints, pull tests, and resistance measurements before and after thermal cycling. The samples were cycled for .ltoreq.20,000 times from -75 to 65.degree. to simulate the temp. environment typically encountered by solar arrays in low earth orbit. The Sn-Ag solder will withstand thermal cycling with minimal degrdn., when compared to the frequency used Sn-Pb-Ag type.

IT ***11144-61-9***
(solders, for solar array ***interconnects*** )
RN 11144-61-9 HCA
CN Silver alloy, nonbase, Ag,Sn (9CI) (CA INDEX NAME)

| Component | Component Registry Number |
|---|---|
| Ag | 7440-22-4 |
| Sn | 7440-31-5 |

CC 52-2 (Electrochemical, Radiational, and Thermal Energy Technology)
Section cross-reference(s): 56
ST solder solar array ***interconnect*** ; ***cell*** ***solar*** array ***interconnect*** solder; tin silver solder solar array; lead tin silver solder array
IT Photoelectric devices, solar
(array of, solders for ***interconnects*** of)
IT Solders
(silver-tin alloy, for solar array ***interconnects*** )
IT ***11144-61-9*** 56925-19-0
(solders, for solar array ***interconnects*** )

=> d his

L28 25 S (NONLEAD? OR NON(N)(LEAD OR LEADEN OR PB))(3N)SOLDER?
L29 0 S L28 AND L5
L30 1 S L28 AND L11
L31 0 S L30 AND L14
L32 0 S L30 AND SOLAR?

=> d l30 1 cbib abs hitstr hitind

L30 ANSWER 1 OF 1 HCA COPYRIGHT 2003 ACS on STN
134:171130 A review of electrically conductive adhesive technology for use in surface-mount microelectronics. Rafanelli, Anthony J. (Naval & Maritime Integrated Systems, ASME International Raytheon Company, Portsmouth, RI, 02871, USA). EEP (American Society of Mechanical Engineers), 28(Packaging of Electronic and Photonic Devices), 197-202 (English) 2000. CODEN: EEAEEM. Publisher: American Society of Mechanical Engineers.

AB Interest in alternatives to lead solders continues to increase due to several initiatives addressing the redn. of lead usage and subsequent exposure to the environment. Alternative materials can be categorized into two main groups: elec. conductive adhesives (polymers) and ***non*** - ***lead*** ***solders*** . Over the past ten years, many non-leaded solders have been developed and introduced to the electronics industry. Despite some success regarding processability, several issues still exist regarding use of these materials as "drop-in" replacements for traditional leaded solders, e.g. eutectic tin-lead. This paper provides an overview of the second alternate material group, i.e. elec. conductive adhesives. An attempt is made to compare the characteristics of these materials to the tin-lead benchmark. A summary of key material properties is also included. Finally, a position is presented regarding the approaches taken in evaluating these materials as suitable substitutes for tin-lead eutectic solder. Focus is on applications in surface mount technol. (SMT) ***interconnection*** since solder is the primary bonding medium for ***interconnections*** . In general, these materials are acceptable for most applications. Applications under harsh service and environmental conditions, however, would require evaluation on a case-by-case basis. Many refs.

CC 76-0 (Electric Phenomena)

DIAL

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?show files
File   2:INSPEC 1969-2003/Aug W3
         (c) 2003 Institution of Electrical Engineers
File 347:JAPIO Oct 1976-2003/Apr(Updated 030804)
         (c) 2003 JPO & JAPIO
File 350:Derwent WPIX 1963-2003/UD,UM &UP=200354
         (c) 2003  Thomson Derwent
?ds

Set      Items   Description
S1       57307   SOLARCELL? OR (SOLAR? OR PHOTOELEC?)(2N)(CELL OR CELLS) OR
             SOLAR?(2N)(PANEL? OR ARRAY?) OR SOLARPANEL? OR SOLARARRAY?
S2        2062   INTERCONNECT?R?
S3      239099   INTERCONNECT?
S4        1863   (LEADFREE? OR (LEAD OR PB)(2N)(FREE? ? OR FREEING? ? OR AB-
             SENT? OR ABSENC? OR WITHOUT? OR LACK? OR NONE OR NONEXIST?))(-
             3N)SOLDER?
S5           2   S2 AND S4
S6         206   S3 AND S4
S7           3   S6 AND S1
S8          48   S3(5N)S4
S9          39   (NONLEAD? OR NON(N)(LEAD OR LEADEN OR PB))(3N)SOLDER?
S10          0   S9 AND S2
S11          1   S9 AND S3
S12          0   S11 AND S1
S13          4   S5 OR S7 OR S11
S14         47   S8 NOT S13
S15          4   RD S13 (unique items)
S16         46   RD S14 (unique items)

?t s15/7,de/all

 15/7,DE/1      (Item 1 from file: 2)
DIALOG(R)File   2:INSPEC
(c) 2003 Institution of Electrical Engineers. All rts. reserv.

7035415   INSPEC Abstract Number: B2001-10-0170Q-003
Title: ISO 14000 introduction in the photovoltaic industry
  Author(s): Rosenblum, M.D.; Brown, R.L.; Gonsiorawski, R.; Kalejs, J.P.
  Author Affiliation: ASE Americas Inc., Billerica, MA, USA
  Conference Title: Conference Record of the Twenty-Eighth IEEE
Photovoltaic Specialists Conference - 2000 (Cat. No.00CH37036)   p.1476-8
  Publisher: IEEE, Piscataway, NJ, USA
  Publication Date: 2000  Country of Publication: USA   xxxii+1838 pp.
  ISBN: 0 7803 5772 8     Material Identity Number: XX-2000-00406
  U.S. Copyright Clearance Center Code: 0 7803 5772 8/2000/$10.00
  Conference Title: Proceedings of 28th IEEE Photovoltaic Specialists
Conference
  Conference Sponsor: IEEE Electron Devices Soc
  Conference Date: 15-22 Sept. 2000   Conference Location: Anchorage, AK,
USA
  Language: English   Document Type: Conference Paper (PA)
  Treatment: Practical (P)
  Abstract: ASE Americas has initiated a program to become certified under
the ISO 14001 environmental management system. Background information is
provided about the ISO 14000 series of standards, along with benefits
resulting from certification. Details specific to the efforts being
undertaken at our facility to become ISO 14001 certified are given. A gap
audit has been conducted to assess our current state of readiness in
advance of the registration process: highlights of the findings are
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presented. We then highlight several processes which have been developed and implemented at ASE to abate the environmental impact of PV manufacturing and address product life cycle concerns. Foremost among these are pioneering work on the use of lead-free solder paste for cell interconnect, and development of new technology to reduce the volume of acids used in manufacturing in the areas of wafer etching/cleaning and phosphorus glass etching. (9 Refs)
Subfile: B
Descriptors: certification; environmental factors; etching; ISO standards ; management; solar cells; soldering; surface cleaning


15/7,DE/2 (Item 2 from file: 2)
DIALOG(R)File 2:INSPEC


4834245 INSPEC Abstract Number: B9501-2210D-026
Title: Material and assembly issues of non-lead bearing solder alloys
Author(s): Melton, C.; Skipor, A.; Thome, J.
Author Affiliation: Motorola, Inc., Schaumburg, IL, USA
p.1489-94 vol.3
Publisher: Reed Exhibition Companies, Des Plaines, IL, USA
Publication Date: 1993 Country of Publication: USA 3 vol. 2022 pp.
Conference Title: Proceedings of NEPCON West
Conference Date: 7-11 Feb. 1993 Conference Location: Anaheim, CA, USA
Language: English Document Type: Conference Paper (PA)
Treatment: Practical (P); Experimental (X)
Abstract: Environmental concerns have prompted recent federal mandates to tax or ban the usage of lead. The potential effect of this legislation on the assembly of electronic components has stirred interest in identifying alternative interconnect materials. This paper discusses solder pastes comprised of non-lead bearing solder alloys with emphasis on current processing changes that might be warranted due to the use of alternative flux/alloy combinations. The main technical issues to be addressed are in the realm of solder wettability, manufacturing process issues and the reliability performance of these materials in electronic assemblies. (10 Refs)
Subfile: B
Descriptors: assembling; circuit reliability; environmental engineering; legislation; packaging; printed circuit manufacture; soldering; wetting

15/7,DE/3 (Item 1 from file: 347)
DIALOG(R)File 347:JAPIO


07348943
SOLAR CELL, INTERCONNECTOR AND STRING FOR THE SOLAR CELL

PUB. NO.: 2002-217434 [JP 2002217434 A] (date no good)
PUBLISHED: August 02, 2002 (20020802)
INVENTOR(s): TANAKA SATOSHI
APPLICANT(s): SHARP CORP
APPL. NO.: 2001-011603 [JP 20011011603]
FILED: January 19, 2001 (20010119)

ABSTRACT

PROBLEM TO BE SOLVED: To provide a solar battery which can maintain proper

cell characteristics and is coated with a lead-free solder which does not contain lead.

SOLUTION: This solar battery includes electrodes 5, 6 which are coated with a lead-free solder which does not contain lead.



15/7,DE/4 (Item 1 from file: 350)
DIALOG(R)File 350:Derwent WPIX


014915532
WPI Acc No: 2002-736239/200280
Solar cell consists of electrodes which are covered by lead free solder layer
Patent Assignee: SHARP KK (SHAF ); TANAKA S (TANA-I)
Inventor: TANAKA S
Number of Countries: 002 Number of Patents: 002
Patent Family:

| Patent No | Kind | Date | Applicat No | Kind | Date | Week | |
|---|---|---|---|---|---|---|---|
| JP 2002217434 | A | 20020802 | JP 200111603 | A | 20010119 | 200280 | B |
| US 20020148499 | A1 | 20021017 | US 200238681 | A | 20020108 | 200281 | |

Priority Applications (No Type Date): JP 200111603 A 20010119
Patent Details:

| Patent No | Kind | Lan | Pg | Main IPC | Filing Notes |
|---|---|---|---|---|---|
| JP 2002217434 | A | | 8 | H01L-031/04 | |
| US 20020148499 | A1 | | | H01L-031/00 | |

Abstract (Basic): JP 2002217434 A
Abstract (Basic):
NOVELTY - The solar cell has silver electrodes (5,6) which are covered by lead free solder layer (8) like Sn-Bi-Ag and Sn-Ag solder.
DETAILED DESCRIPTION - INDEPENDENT CLAIMS are included for the following:
(1) Interconnector for solar cell;and
(2) String.
USE - Solar cell.
ADVANTAGE - Obtains favorable cell characteristics without environmental problems.
DESCRIPTION OF DRAWING(S) - The figure shows the sectional drawing of the solar cell.
Silver electrodes (5,6)
Lead free solder layers (8)
pp; 8 DwgNo 4/5
Title Terms: SOLAR; CELL; CONSIST; ELECTRODE; COVER; LEAD; FREE; SOLDER; LAYER
Derwent Class: L03; M26; P55; U11; U12; X15
International Patent Class (Main): H01L-031/00; H01L-031/04
International Patent Class (Additional): B23K-001/00; B23K-001/20; B23K-035/26

?t s16/ti/all

↓↓↓ (non-solar art)

16/TI/1 (Item 1 from file: 2)
DIALOG(R)File 2:(c) 2003 Institution of Electrical Engineers. All rts. reserv.

Title: An assessment of lead free solder (Sn3.7Ag0.8Cu) wettability

16/TI/2 (Item 2 from file: 2)
DIALOG(R)File 2:(c) 2003 Institution of Electrical Engineers. All rts. reserv.

Title: Controllability of novel Sn/sub 0.95/Au/sub 0.05/ microbumps using interlaminated tin and gold layers for flip-chip interconnection

16/TI/3 (Item 3 from file: 2)
DIALOG(R)File 2:(c) 2003 Institution of Electrical Engineers. All rts. reserv.

Title: Lead free interconnection technology and the environment

16/TI/4 (Item 4 from file: 2)
DIALOG(R)File 2:(c) 2003 Institution of Electrical Engineers. All rts. reserv.

Title: Time-independent mechanical and physical properties of the ternary 95.5Sn-3.9Ag-0.6Cu solder

16/TI/5 (Item 5 from file: 2)
DIALOG(R)File 2:(c) 2003 Institution of Electrical Engineers. All rts. reserv.

Title: Characterization of the reaction process in diffusion-soldered Cu/In-48 at.% Sn/Cu joints

16/TI/6 (Item 6 from file: 2)
DIALOG(R)File 2:(c) 2003 Institution of Electrical Engineers. All rts. reserv.

Title: Challenges and opportunities in lead-free solder PCB assembly

16/TI/7 (Item 7 from file: 2)
DIALOG(R)File 2:(c) 2003 Institution of Electrical Engineers. All rts. reserv.

Title: Pressfit technology for 3-D molded interconnect devices (MID) - A lead-free alternative to solder joints - challenges and solutions concepts

16/TI/8 (Item 8 from file: 2)
DIALOG(R)File 2:(c) 2003 Institution of Electrical Engineers. All rts. reserv.

Title: Lead-free solder bump technologies for flip-chip electronic packaging applications

16/TI/9 (Item 9 from file: 2)
DIALOG(R)File 2:(c) 2003 Institution of Electrical Engineers. All rts. reserv.

Title: Novel flip-chip bonding technology for W-band interconnections using alternate lead-free solder bumps

16/TI/10 (Item 10 from file: 2)
DIALOG(R)File 2:(c) 2003 Institution of Electrical Engineers. All rts. reserv.

Title: Lead-free solder bump technologies for flip-chip packaging applications

16/TI/11 (Item 11 from file: 2)
DIALOG(R)File 2:(c) 2003 Institution of Electrical Engineers. All rts. reserv.

Title: Reliability evaluations of chip interconnect in lead-free solder systems

16/TI/12 (Item 12 from file: 2)
DIALOG(R)File 2:(c) 2003 Institution of Electrical Engineers. All rts. reserv.

Title: Reliability assessment of flip-chip assemblies with lead-free solder joints

16/TI/13 (Item 13 from file: 2)
DIALOG(R)File 2:(c) 2003 Institution of Electrical Engineers. All rts. reserv.

Title: Solder joint reliability and characteristics of deformation and crack growth of Sn-Ag-Cu versus eutectic Sn-Pb on a WLP in a thermal cycling test

16/TI/14 (Item 14 from file: 2)
DIALOG(R)File 2:(c) 2003 Institution of Electrical Engineers. All rts. reserv.

Title: Thermo-mechanical reliability of lead-free solder interconnects

16/TI/15 (Item 15 from file: 2)
DIALOG(R)File 2:(c) 2003 Institution of Electrical Engineers. All rts. reserv.

Title: Board level reliability of lead-free soldered interconnects on conventional and area array components

16/TI/16 (Item 16 from file: 2)
DIALOG(R)File 2:(c) 2003 Institution of Electrical Engineers. All rts. reserv.

Title: Reliability of lead-free solder interconnects-a review

16/TI/17 (Item 17 from file: 2)

DIALOG(R)File 2:(c) 2003 Institution of Electrical Engineers. All rts. reserv.

Title: Flip chip with lead-free solders on halogen-free microvia substrates

16/TI/18 (Item 18 from file: 2)
DIALOG(R)File 2:(c) 2003 Institution of Electrical Engineers. All rts. reserv.

Title: Constitutive behaviour of lead-free solders vs. lead-containing solders-experiments on bulk specimens and flip-chip joints

16/TI/19 (Item 19 from file: 2)
DIALOG(R)File 2:(c) 2003 Institution of Electrical Engineers. All rts. reserv.

Title: Wafer level interconnects with lead-free and low alpha solders

16/TI/20 (Item 20 from file: 2)
DIALOG(R)File 2:(c) 2003 Institution of Electrical Engineers. All rts. reserv.

Title: Board level reliability of lead free soldered interconnections

16/TI/21 (Item 21 from file: 2)
DIALOG(R)File 2:(c) 2003 Institution of Electrical Engineers. All rts. reserv.

Title: Pb-free solders for flip-chip interconnects

16/TI/22 (Item 22 from file: 2)
DIALOG(R)File 2:(c) 2003 Institution of Electrical Engineers. All rts. reserv.

Title: Interfacial embrittlement by bismuth segregation in copper/tin-bismuth Pb-free solder interconnect

16/TI/23 (Item 23 from file: 2)
DIALOG(R)File 2:(c) 2003 Institution of Electrical Engineers. All rts. reserv.

Title: Calculation of phase equilibria in candidate solder alloys

16/TI/24 (Item 24 from file: 2)
DIALOG(R)File 2:(c) 2003 Institution of Electrical Engineers. All rts. reserv.

Title: Improvement in thermal reliability of a flip chip interconnection system joined by Pb-free solder and Au bumps

16/TI/25 (Item 25 from file: 2)

DIALOG(R)File 2:(c) 2003 Institution of Electrical Engineers. All rts. reserv.

Title: Thermo-mechanical properties and creep deformation of lead-containing and lead-free solders

16/TI/26 (Item 26 from file: 2)
DIALOG(R)File 2:(c) 2003 Institution of Electrical Engineers. All rts. reserv.

Title: Lead-free flip chip processing with halogen-free high density microvia substrates

16/TI/27 (Item 27 from file: 2)
DIALOG(R)File 2:(c) 2003 Institution of Electrical Engineers. All rts. reserv.

Title: Lead free soldering electronic interconnect: Current status and future developments

16/TI/28 (Item 28 from file: 2)
DIALOG(R)File 2:(c) 2003 Institution of Electrical Engineers. All rts. reserv.

Title: Flip chip processing of lead-free solders and halogen-free high density microvia substrates

16/TI/29 (Item 29 from file: 2)
DIALOG(R)File 2:(c) 2003 Institution of Electrical Engineers. All rts. reserv.

Title: 2000 Proceedings. 50th Electronic Components and Technology Conference (Cat. No.00CH37070)

16/TI/30 (Item 30 from file: 2)
DIALOG(R)File 2:(c) 2003 Institution of Electrical Engineers. All rts. reserv.

Title: SMTA International. Proceedings of Technical Program. Conference Proceedings

16/TI/31 (Item 31 from file: 2)
DIALOG(R)File 2:(c) 2003 Institution of Electrical Engineers. All rts. reserv.

Title: A novel flip chip bonding technology using Au stud bump and lead-free solder

16/TI/32 (Item 32 from file: 2)
DIALOG(R)File 2:(c) 2003 Institution of Electrical Engineers. All rts. reserv.

Title: Deformation behavior of two lead-free solders

16/TI/33 (Item 33 from file: 2)
DIALOG(R)File 2:(c) 2003 Institution of Electrical Engineers. All rts. reserv.

Title: Reliability assessment of BGA interconnects with CADMP-II

16/TI/34 (Item 34 from file: 2)
DIALOG(R)File 2:(c) 2003 Institution of Electrical Engineers. All rts. reserv.

Title: Tin-silver-copper: a lead free solder for capacitor interconnects

16/TI/35 (Item 35 from file: 2)
DIALOG(R)File 2:(c) 2003 Institution of Electrical Engineers. All rts. reserv.

Title: Assessment of circuit board surface finishes for electronic assembly with lead-free solders

16/TI/36 (Item 36 from file: 2)
DIALOG(R)File 2:(c) 2003 Institution of Electrical Engineers. All rts. reserv.

Title: Printed wiring board surface finishes: evaluation of electroless noble metal coatings

16/TI/37 (Item 37 from file: 2)
DIALOG(R)File 2:(c) 2003 Institution of Electrical Engineers. All rts. reserv.

Title: Lead free interconnect materials for the electronics industry

16/TI/38 (Item 38 from file: 2)
DIALOG(R)File 2:(c) 2003 Institution of Electrical Engineers. All rts. reserv.

Title: NCMS lead elimination programs for the electronic interconnect industry

16/TI/39 (Item 39 from file: 2)
DIALOG(R)File 2:(c) 2003 Institution of Electrical Engineers. All rts. reserv.

Title: Alternatives of lead bearing solder alloys

16/TI/40 (Item 1 from file: 347)
DIALOG(R)File 347:(c) 2003 JPO & JAPIO. All rts. reserv.

COOLED TYPE PHOTOELECTRIC CONVERSION DEVICE

16/TI/41 (Item 1 from file: 350)
DIALOG(R)File 350:(c) 2003 Thomson Derwent. All rts. reserv.

Electronic components separation method for removing chips from circuit board involves positioning heated element adjacent to solder interconnections, such that elements engages, cuts through and severs interconnection

16/TI/42 (Item 2 from file: 350)
DIALOG(R)File 350:(c) 2003 Thomson Derwent. All rts. reserv.

Substrate interconnection method for ball grid array, involves heating spaced substrates to predetermined temperature, to melt their respective solder balls and solder pads into single reflowed solder ball

16/TI/43 (Item 3 from file: 350)
DIALOG(R)File 350:(c) 2003 Thomson Derwent. All rts. reserv.

Solder interconnect structure for electronic package, has joiner interconnect with lead-free joiner solder whose liquidus temperature is less than solidus temperature of lead-free core solder of core interconnect

16/TI/44 (Item 4 from file: 350)
DIALOG(R)File 350:(c) 2003 Thomson Derwent. All rts. reserv.

Electronic structure, for use in forming electronic package, includes interconnect structures comprising joiner solder and core solder that are lead free

16/TI/45 (Item 5 from file: 350)
DIALOG(R)File 350:(c) 2003 Thomson Derwent. All rts. reserv.

Lead-free solder alloy for use in solder interconnections in microelectronics and electronic applications has preset liquidus melting temperature and includes tin, copper, silver and indium

16/TI/46 (Item 6 from file: 350)
DIALOG(R)File 350:(c) 2003 Thomson Derwent. All rts. reserv.

Lead-free solder alloy for soldering interconnections in microelectronics and electronics applications comprises tin, copper, silver, and indium

?t s16/7,de/1,3,4,6,8,9,10,11,14,15,16,17,19,20,21,22,27,34,37,39,40,43,44,45,46

16/7,DE/1 (Item 1 from file: 2)
DIALOG(R)File 2:INSPEC
(c) 2003 Institution of Electrical Engineers. All rts. reserv.

7712515 INSPEC Abstract Number: B2003-09-2210D-014
Title: An assessment of lead free solder (Sn3.7Ag0.8Cu) wettability
Author(s): Key Chung, C.; Mustapha, F.; Hua, F.; Aspandiar, R.
Author Affiliation: Manuf. Technol. Manuf. Malaysia, Kulim, Malaysia
Conference Title: Proceedings 4th Electronics Packaging Technology Conference (EPTC 2002) (Cat. No.02EX566) p.1-5

Editor(s): Lee, C.; Chuan, T.K.; Iyer, M.K.
Publisher: IEEE, Piscataway, NJ,USA
Publication Date: 2002 Country of Publication: USA 453 pp.
ISBN: 0 7803 7435 5 Material Identity Number: XX-2003-00270
U.S. Copyright Clearance Center Code: 0-7803-7435-5/02/$17.00
Conference Title: Proceedings 4th Electronics Packaging Technology Conference (EPTC 2002)
Conference Date: 10-12 Dec. 2002 Conference Location: Singapore
Language: English Document Type: Conference Paper (PA)
Treatment: Practical (P); Experimental (X)
Abstract: The National Electronics Manufacturing Initiative (NEMI) standardized lead free solder tin/silver/copper (SnAgCu) ternary system in January 2000. This Sn3.7Ag0.8Cu has higher melting temperature of 217 degrees C as compared with current eutectic tin/lead solder (63Sn/37Pb; 183 degrees C). Thus, it is a challenge to electronic lead free packaging that requires higher reflow temperature. Optimizing lead-free-reflow-soldering process in second level interconnection is a critical step to ensure reliable solder joint is properly manufactured. This paper presents the assessment of lead free solder wettability. It covers a wide range of soldering parameters with 4 dominant factors and 14 variables. They are 4 different printed circuit board surface coatings (organic surface preservative, OSP; immersion silver, ImAg; electroless nickel immersion gold, ENIG and tin/lead hot air solder leveling), 4 different fluxes in SnAgCu solder pastes, 3 different reflow peak temperatures (225 degrees C, 230 degrees C and 235 degrees C) and 3 different ranges of time above liquidous (30-60s, 60-90s and 120-150s). A test board is designed in these studies. Wetting angles are output parameters and measured using a noncontact laser measurement system. (14 Refs)
Subfile: B
Descriptors: copper alloys; electroless deposition; measurement by laser beam; packaging; printed circuit manufacture; reflow soldering; silver alloys; tin alloys; wetting


16/7,DE/3 (Item 3 from file: 2)
DIALOG(R)File 2:INSPEC


7703730 INSPEC Abstract Number: B2003-09-2550F-013
Title: Lead free interconnection technology and the environment
Author(s): Mueller, J.; Griese, H.; Reichl, H.; Zuber, K.-H.
Author Affiliation: Fraunhofer Inst. for Reliability & Microintegration, Berlin, Germany
Conference Title: 38th International Conference on Microelectronics, Devices and Materials and the Workshop on Packaging and Interconnections in Electronics. Proceedings p.47-56
Editor(s): Kosec, M.; Belavic, D.; Sorli, I.
Publisher: MIDEM - Soc. Microelectron., Electron. Components & Mater, Ljubljana, Slovenia
Publication Date: 2002 Country of Publication: Slovenia x+378 pp.
ISBN: 961 91023 0 4 Material Identity Number: XX-2002-03486
Conference Title: 38th International Conference on Microelectronics, Devices and Materials
Conference Sponsor: Ministr. Educ., Sci. & Sport; HIPOT-HYB Production of Hybird Circuits; IMAPS; IEEE Slovenia
Conference Date: 9-11 Oct. 2002 Conference Location: Lipica, Slovenia
Language: English Document Type: Conference Paper (PA)
Treatment: Practical (P)
Abstract: Trends of growing consumption, decreasing product lifetime and

new application fields in nearly all industry segments lead to an enormous increase of electronics products. The production of raw materials and products, their use as well as the end of life treatment of these products cause considerable environmental impacts. To minimise hazards to human health and the environment, an economic growth in a sense of sustainable development has to be realised and new products and process technologies should proof that they contribute to the solution of global environmental issues. In this paper the interconnection technologies as key technologies for future products ore discussed in correlation to their environmental behaviour. At the present a transition to lead free soldering takes place worldwide. In that respect various environmental aspects of the different lead free interconnection systems (solders and surface finishes) should be compared in order to find the best solution from an ecological point of view. (4 Refs)
Subfile: B
Descriptors: environmental factors; integrated circuit interconnections; soldering; surface treatment


16/7,DE/4 (Item 4 from file: 2)
DIALOG(R)File 2:INSPEC


7619643 INSPEC Abstract Number: A2003-12-8140L-241, B2003-06-0170G-016
Title: Time-independent mechanical and physical properties of the ternary 95.5Sn-3.9Ag-0.6Cu solder
Author(s): Vianco, P.T.; Rejent, J.A.; Kilgo, A.C.
Author Affiliation: Sandia Nat. Labs., Albuquerque, NM, USA
Journal: Journal of Electronic Materials vol.32, no.3 p.142-51
Publisher: TMS; IEEE,
Publication Date: March 2003 Country of Publication: USA
CODEN: JECMA5 ISSN: 0361-5235
SICI: 0361-5235(200303)32:3L.142:TIMP;1-U
Material Identity Number: J246-2003-005
U.S. Copyright Clearance Center Code: 0361-5235/03/$7.00
Language: English Document Type: Journal Paper (JP)
Treatment: Practical (P); Experimental (X)
Abstract: The development of a constitutive model for predicting the thermal-mechanical fatigue (TMF) of 95.5Sn-3.9Ag-0.6Cu (wt.%) Pb-free solder interconnects requires the measurement of time-independent mechanical and physical properties. Yield stress was measured over the temperature range of -25-160 degrees C using strain rates of 4.2 * 10/sup -5/ s/sup -1/ and 8.3 * 10/sup -4/ s/sup -1/. The yield-stress values ranged from approximately 40 MPa at -25 degrees C to 10 MPa at 160 degrees C for tests performed at 4.2 * 10/sup -5/ s/sup -1/. The faster strain rate and specimen aging had a limited impact on the yield stress. The true stress/true strain curves indicated that dynamic-recovery and dynamic-recrystallization processes took place in as-cast samples exposed to temperatures of 125 degrees C and 160 degrees C, respectively, while tested at a strain rate of 4.2 * 10/sup -5/ s/sup -1/. Aging the sample prior to testing, as well as a faster strain rate, mitigated both phenomena. Dynamic Young's modulus values ranged from 55 GPa at -50 degrees C to 35 GPa at 200 degrees C, while the coefficient of thermal expansion (CTE) increased from approximately 12 * 10/sup -6/ degrees C/sup -1/ to 24 * 10/sup -6/ degrees C/sup -1/ for the same temperature range. The aging treatment had little effect on either Young's modulus or the CTE. (9 Refs)
Subfile: A B
Descriptors: ageing; copper alloys; fatigue; integrated circuit interconnections; recrystallisation; silver alloys; soldering;

stress-strain relations; thermal expansion; tin alloys; work hardening; yield stress; Young's modulus
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16/7,DE/6 (Item 6 from file: 2)
DIALOG(R)File 2:INSPEC


7519552 INSPEC Abstract Number: B2003-03-2210D-017
Title: Challenges and opportunities in lead-free solder PCB assembly
Author(s): Shangguan, D.
Author Affiliation: Flextronics, CA, USA
Journal: Global SMT & Packaging vol.2, no.7 p.18-24
Publisher: Trafalgar Publications Ltd,
Publication Date: Oct. 2002 Country of Publication: UK
CODEN: GSPLAU ISSN: 1474-0893
SICI: 1474-0893(200210)2:7L.18:COLF;1-L
Material Identity Number: H786-2002-008
Language: English Document Type: Journal Paper (JP)
Treatment: General, Review (G); Practical (P)
Abstract: This paper is an overview of the issues involved in lead-free solder PCB assembly, including solder alloy characteristics, metallurgical interactions and compatibility, solder paste requirements, and impact on PCB and components. Electrochemical and mechanical reliability issues for lead-free solder interconnects are discussed. Process development for lead-free soldering is discussed for reflow, wave soldering, and rework. Quality, equipment, cost, and design issues are also reviewed. The transition to lead-free soldering needs to be carefully managed, and industry-wide cooperation is critical to achieving a smooth transition. ( 22 Refs)
Subfile: B
Descriptors: assembling; circuit reliability; interconnections; printed circuit manufacture; reflow soldering; wave soldering


16/7,DE/8 (Item 8 from file: 2)
DIALOG(R)File 2:INSPEC


7447327 INSPEC Abstract Number: B2002-12-0170J-149
Title: Lead-free solder bump technologies for flip-chip electronic packaging applications
Author(s): Karim, Z.S.; Chow, A.; Cheung, E.; Cheung, G.
Author Affiliation: Adv. Interconnect Technol. Ltd., Tsuen Wan, China
Conference Title: Proceedings of the Eleventh International Workshop on the Physics of Semiconductor Devices (SPIE Vol.4746) Part vol.1 p. 570-5 vol.1
Editor(s): Kumar, V.; Basu, P.K.
Publisher: SPIE, Washington, DC, USA
Publication Date: 2002 Country of Publication: USA 2 vol.(xxxix+xl+1460) pp.
ISBN: 0 8194 4500 2 Material Identity Number: XX-2002-02457
Conference Title: Proceedings of the Eleventh International Workshop on the Physics of Semiconductor Devices
Conference Sponsor: Defence Res. & Dev. Organ.; Ministr. Inf. Technol.; Dept. Sci. & Technol.; et al
Conference Date: 11-15 Dec. 2001 Conference Location: Delhi, India
Language: English Document Type: Conference Paper (PA)

Treatment: Practical (P); Experimental (X)
Abstract: We describe the fabrication and characterization of five different types of lead-free solder bump interconnections for use in various flip-chip electronic packaging applications. Lead-free solder bumps were fabricated from pure-tin (Sn), tin-bismuth (Sn:Bi), eutectic tin-copper (Sn:Cu), eutectic tin-silver (Sn:Ag), and ternary tin-silver-copper (Sn:Ag:Cu) alloys. The fabrication process consisted of electrolytic plating, using a fountain (cup) plater, of a 5 mu m thick copper under-bump-metal (UBM) onto which was plated the lead-free solder bump. The as-plated bumps were subsequently re-flowed in a 5-zone re-flow oven. Due to the characteristic high-tin compositions of the lead-free solder alloys, which can cause the rapid and uneven formation of tin-copper intermetallics at the bump-UBM interface upon re-flow, a unique proprietary nickel "cap" using a single photolithography process that completely encapsulates the copper UBM was developed. Two different test structures, one with perimeter- and a second with area-distributed solder bumps, each with bumps of average size 125 mu m diameter (post-re-flow) were fabricated onto "daisy-chain" wafers to characterize the lead-free solder bumping and bonding processes and to conduct a series of reliability tests. Characterization of the properties of the lead-free bumps included the use of Scanning Electron Microscopy (SEM), Energy Dispersive X-ray (EDX), Auger Electron Spectroscopy (AES), micro-sectioning, and ball shear measurements for which the bumps were re-flowed multiple times and subjected to ball shear tests in-between re-flows to study the formation of intermetallic compounds. Lead-free solder bumped "daisy-chain" test die were also flip-chip bonded onto BT-epoxy substrates with patterned copper traces overplated with nickel/gold. The bonded die were underfilled and subjected to environmental tests consisting high-temperature storage, thermal cycling, and accelerated aging. Details of the lead-free solder bump fabrication process together with the performance results including their electrical, mechanical, and reliability characteristics will be presented for all five lead-free alloys chosen in this study. (4 Refs)
Subfile: B
Descriptors: Auger electron spectra; flip-chip devices; integrated circuit interconnections; integrated circuit reliability; reflow soldering; scanning electron microscopy; semiconductor device packaging; tin alloys; X-ray chemical analysis


16/7,DE/9 (Item 9 from file: 2)
DIALOG(R)File 2:INSPEC


7429687 INSPEC Abstract Number: B2002-12-2240-005
Title: Novel flip-chip bonding technology for W-band interconnections using alternate lead-free solder bumps
Author(s): Onodera, K.; Ishii, T.; Aoyama, S.; Sugitani, S.; Tokumitsu, M.
Author Affiliation: Photonics Labs., NTT Corp., Kanagawa, Japan
Journal: IEEE Microwave and Wireless Components Letters vol.12, no.10 p.372-4
Publisher: IEEE,
Publication Date: Oct. 2002 Country of Publication: USA
CODEN: IMWCBJ ISSN: 1531-1309
SICI: 1531-1309(200210)12:10L.372:NFCB;1-J
Material Identity Number: J683-2002-011
U.S. Copyright Clearance Center Code: 1531-1309/02/$17.00
Language: English Document Type: Journal Paper (JP)
Treatment: New Developments (N); Practical (P); Experimental (X)

Abstract: A novel lead-free flip-chip technology for mounting high-speed compound semiconductor ICs, which have a relatively severe limitation regarding high-heat treatment, is presented. Solder bump interconnections of 0.95Sn-0.05Au were successfully fabricated by reflowing multilayer metal film at as low a temperature as 220 degrees C. The bumps were designed to have a diameter of 36 mu m with a gap between the chip and the motherboard of 24 mu m. The electrical characteristics of flip-chip-mounted coplanar waveguide chips were measured. The deterioration in reflection loss in the flip chip mounting was less than 3 dB for frequencies up to W-band. (7 Refs)

Subfile: B

Descriptors: coplanar waveguides; flip-chip devices; gold alloys; high-speed integrated circuits; integrated circuit bonding; integrated circuit interconnections; microwave integrated circuits; millimetre wave integrated circuits; reflow soldering; tin alloys



16/7,DE/10 (Item 10 from file: 2)
DIALOG(R)File 2:INSPEC


7411416 INSPEC Abstract Number: B2002-11-0170J-164

Title: Lead-free solder bump technologies for flip-chip packaging applications

Author(s): Karim, Z.S.; Martin, J.

Author Affiliation: Adv. Interconnect Technol. Ltd, Hong Kong, China

Conference Title: Proceedings 2001 International Symposium on Microelectronics (SPIE Vol.4587) p.581-7

Publisher: IMAPS - Int. Microelectron. & Packaging Soc, Washington, DC, USA

Publication Date: 2001 Country of Publication: USA xix+782 pp.

ISBN: 0 930815 64 5 Material Identity Number: XX-2002-00865

Conference Title: 2001 International Symposium on Microelectronics

Conference Sponsor: IMAPS - Int. Microelectron. & Packaging Soc

Conference Date: 9-11 Oct. 2001 Conference Location: Baltimore, MD, USA

Language: English Document Type: Conference Paper (PA)

Treatment: Applications (A); Practical (P); Experimental (X)

Abstract: Describes the fabrication and characterization of five different types of lead-free solder bump interconnections for use in flip-chip electronic packaging applications. Lead-free solder bumps were fabricated from pure-tin (Sn), tin-bismuth (Sn:Bi), eutectic tin-copper (Sn:Cu), eutectic tin-silver (Sn:Ag), and ternary tin-silver-copper (Sn:Ag:Cu) alloys. The fabrication process consists of the electrolytic plating, using a fountain (cup) plater, of a 5 mu m thick copper under-bump-metal (UBM) onto which is plated the lead-free solder. The as-plated bumps were subsequently re-flowed in a 5-zone reflow oven. A unique proprietary nickel "cap" using a single photolithography process that completely encapsulates the copper UBM was developed. Two different test structures, one with perimeter- and a second with area-distributed solder bumps, each with bumps of average size 125 mu m diameter (post-re-flow) were fabricated onto "daisy-chain" wafers to characterize the lead-free solder bumping and bonding process and to conduct a series of reliability tests. (4 Refs)

Subfile: B

Descriptors: electroplating; flip-chip devices; integrated circuit packaging; integrated circuit reliability; photolithography; reflow soldering

16/7,DE/11 (Item 11 from file: 2)
DIALOG(R)File 2:INSPEC


7394932 INSPEC Abstract Number: B2002-11-2550F-014
Title: Reliability evaluations of chip interconnect in lead-free solder systems
Author(s): Yifan Guo; Jong-Kai Lin; Anada De Silva
Author Affiliation: Final Manuf. Technol. Center, Motorola Inc., Tempe, AZ, USA
Conference Title: 52nd Electronic Components and Technology Conference 2002. (Cat. No.02CH37345) p.1275-80
Publisher: IEEE, Piscataway, NJ, USA
Publication Date: 2002 Country of Publication: USA xxxiv+1789 pp.
ISBN: 0 7803 7430 4 Material Identity Number: XX-2002-01381
U.S. Copyright Clearance Center Code: 0-7803-7430-4/02/$17.00
Conference Title: Proceedings of 52nd Electronic Components and Technology Conference
Conference Sponsor: IEEE Components, Packaging, & Manuf. Technol. Soc.; Electronic Components, Assemblies & Mater. Assoc
Conference Date: 28-31 May 2002 Conference Location: San Diego, CA, USA
Medium: Also available on CD-ROM in PDF format
Language: English Document Type: Conference Paper (PA)
Treatment: Practical (P); Experimental (X)
Abstract: Chip interconnect (solder to silicon) reliability is one of the critical elements in the qualification of flip-chip bumping technology. Since the interconnect materials, structures and processes vary in different bumping technologies, the strength and reliability must be evaluated for each design. As lead-free solders are used in the system, the intermetallics associated with the lead-free solders and the UBM (under bump metallurgy) has also influence on the interconnect reliability. In addition, the stress that an interconnect experiences during thermal cycling depends on the properties of the solder alloy used in the interconnect. Different solder alloys require different interconnect strengths to achieve good reliability in thermal cycling. This paper reports on a study of interconnect reliability by comparing the interconnect strength and the working stress in the interconnect during qualification and application. A simple stress model was developed to determine the interconnect stress during thermal cycling. A testing methodology was established for determining the interconnect strength. In this report, the reliability of several interconnect structures in several lead-free solder systems, including Sn/Ag, Sn/Ag/Cu and Sn/Cu solders and the Ni-Au and TiW-Cu UBMs were studied. (4 Refs)
Subfile: B
Descriptors: chip scale packaging; copper alloys; failure analysis; flip-chip devices; integrated circuit bonding; integrated circuit interconnections; integrated circuit packaging; integrated circuit reliability; integrated circuit testing; reflow soldering; silver alloys; thermal stresses; tin alloys


16/7,DE/14 (Item 14 from file: 2)
DIALOG(R)File 2:INSPEC


7335665 INSPEC Abstract Number: B2002-09-0170J-049

Title: Thermo-mechanical reliability of lead-free solder interconnects
Author(s): Schubert, A.; Dudek, R.; Doring, R.; Walter, H.; Auerswald, E. ; Gollhardt, A.; Michel, B.
Author Affiliation: Fraunhofer Inst. for Reliability & Microintegration, Berlin, Germany
Conference Title: 2002 Proceedings. 8th International Advanced Packaging Materials Symposium (Cat. No.02TH8617) p.90-6
Publisher: IEEE, Piscataway, NJ, USA
Publication Date: 2002 Country of Publication: USA xvi+379 pp.
ISBN: 0 7803 7434 7 Material Identity Number: XX-2002-00851
U.S. Copyright Clearance Center Code: 0-7803-7434-7/02/$17.00
Conference Title: 2002 8th International Advanced Packaging Materials Symposium
Conference Sponsor: IEEE Components, Packaging & Manuf. Technol. (CPMT) Packaging Res. Centr at Georgia Tech (USA); Fraunhofer IZM (Germany); Mater. Res. Soc
Conference Date: 3-6 March 2002 Conference Location: Stone Mountain, GA, USA
Language: English Document Type: Conference Paper (PA)
Treatment: Theoretical (T); Experimental (X)
Abstract: Lead-free solder for electronic assemblies and systems is fast becoming a reality primarily because of market driven forces. While the industry has identified possible alternatives to SnPb solder, much work still needs to be done, especially in the following areas: solder materials characterization (temperature and stress dependent inelastic behavior creep and stress relaxation, bulk versus joint behavior), failure mechanisms related to the solder joints of the new alloys (will creep deformation still play a dominant role for e.g. thermally induced low cycle fatigue?), temperature cycle data, for instance, on real components (acceleration factors may depend on accelerated test conditions and solder alloys, and field conditions may be much more benign than accelerated test conditions), life prediction models (models have to incorporate time and temperature dependent behavior of solders, implementation of constitutive equation in FEA software is one of the keys, isothermal fatigue data should not be useful for life prediction model development), solder-surface interactions (solder reacts with metallization to form interfacial intermetallics, intermetallics grow with time and temperature, metallization consumption by intermetallic growth, intermetallics within the solder, thermo-mechanical properties of the intermetallics), and assembly process development. The impact of some of these issues on the reliability assessment of lead-free solder interconnects through experiments and FE calculations is discussed in the paper, shown on examples like SMD-components and Flip-Chips. (8 Refs)
Subfile: B
Descriptors: environmental factors; finite element analysis; flip-chip devices; reliability; soldering; surface mount technology


16/7,DE/15 (Item 15 from file: 2)
DIALOG(R)File 2:INSPEC


7334770 INSPEC Abstract Number: B2002-09-0170J-029
Title: Board level reliability of lead-free soldered interconnects on conventional and area array components
Author(s): Albrecht, H.J.; Wilke, K.
Author Affiliation: Siemens AG, Berlin, Germany
Conference Title: SMTA International. Proceedings of the Technical Program p.409-16

Publisher: Surface Mount Technol. Assoc, Edina, MN, USA
Publication Date: 2001 Country of Publication: USA 878 pp.
Material Identity Number: XX-2001-01534
Conference Title: Proceedings of SMTA International
Conference Date: 30 Sept.-4 Oct. 2001 Conference Location: Rosemont, IL, USA
Medium: Also available on CD-ROM in PDF format
Language: English Document Type: Conference Paper (PA)
Treatment: Applications (A); Practical (P); Experimental (X)
Abstract: In this paper, environmentally benign solders were discussed related to the ability of interaction to different surface finishes on package and board side, investigated for compatibility with existing process parameters and to describe the board level reliability compared to conventional solder materials. The material selection is done based on the results of the European Ideals Project and the further demands to implement lead-free solders successfully (lead-free, low melting, high fatigue resistant for extended applications under the operating point of view). Including the Ideals activities, SnAgCu alloys (pastes) were tested relating to wetting, spreading, dissolution, reflow profile optimization, 3-dimensional defects in comparison with organic vehicles used in the solder paste, interaction with conventional and lead-free finishes on package and board side, and intermetallic formation and fatigue properties. With the pressure of green assemblies, one of the challenges is to select and analyse an alternative solder alloy that is manufacturable (as powder as well as bath solder), cost effective, available, and reliable compared to conventional solder alloys. (14 Refs)
Subfile: B
Descriptors: circuit reliability; fatigue; melting; packaging; printed circuit manufacture; reflow soldering; wetting


16/7,DE/16 (Item 16 from file: 2)
DIALOG(R)File 2:INSPEC


7225533 INSPEC Abstract Number: B2002-05-0170G-001
Title: Reliability of lead-free solder interconnects-a review
Author(s): Tonapi, S.; Gopakumar, S.; Borgesen, P.; Srihari, K.
Author Affiliation: GE Corporate Res. & Dev., Albany, NY, USA
Conference Title: Annual Reliability and Maintainability Symposium. 2002 Proceedings (Cat. No.02CH37318) p.423-8
Publisher: IEEE, Piscataway, NJ, USA
Publication Date: 2002 Country of Publication: USA xxiv+658 pp.
ISBN: 0 7803 7348 0 Material Identity Number: XX-2001-00557
U.S. Copyright Clearance Center Code: 0-7803-7348-0/02/$10.00
Conference Title: Proceedings of 2002 Annual Reliability and Maintainability Symposium (RAMS)
Conference Date: 28-31 Jan. 2002 Conference Location: Seattle, WA, USA
Language: English Document Type: Conference Paper (PA)
Treatment: General, Review (G)
Abstract: This paper discusses reliability issues related to lead-free printed circuit board interconnects. A comprehensive review of the published literature was carried out, and complemented further by reliability experiments that have been conducted to understand the behavior of some of the lead-free alternatives. The failure mechanisms for lead-free flip chips during accelerated testing are discussed. Some of the metallurgical effects due to the change in soldering system are also reviewed. In the case of assembly of lead-free flip chips, solder joint properties were still found to depend on the reflow profile (peak

temperature and time above the liquidus temperature). The ultimate shear strength of Sn/Ag/Cu (SAC) joints on Ni/Au-coated substrate pads proved very sensitive to small changes in peak temperature and time above liquidus. A similar effect was not observed on Cu/OSP pads. The reflow profile with a lower peak temperature and a lower time above the liquidus temperature gave slightly lower shear strength of joints between two Ni-pads, while the profile with a higher peak temperature and a higher time above the liquidus gave a considerably higher strength. Not surprisingly, the fatigue resistance of both encapsulated and nonencapsulated Sn/Ag/Cu joints was significantly lower on Ni/Au-pads than on Cu/OSP. (15 Refs)
Subfile: B
Descriptors: circuit testing; packaging; printed circuit testing; reliability; reviews; shear strength; soldering


16/7,DE/17 (Item 17 from file: 2)
DIALOG(R)File 2:INSPEC


7062259 INSPEC Abstract Number: B2001-11-0170J-211
Title: Flip chip with lead-free solders on halogen-free microvia substrates
Author(s): Baynham, G.; Baldwin, D.F.; Boustedt, K.; Wennerholm, C.
Author Affiliation: George W. Woodruff Sch. of Mech. Eng., Georgia Inst. of Technol., Atlanta, GA, USA
Conference Title: 2001 Proceedings. 51st Electronic Components and Technology Conference (Cat. No.01CH37220) p.1135-9
Publisher: IEEE, Piscataway, NJ, USA
Publication Date: 2001 Country of Publication: USA xxxiii+1518 pp.
ISBN: 0 7803 7038 4 Material Identity Number: XX-2001-01138
U.S. Copyright Clearance Center Code: 0 7803 7038 4/2001/$10.00
Conference Title: 51st Electronic Components and Technology Conference 2001. Proceedings
Conference Sponsor: Components, Packaging, & Manuf. Technol. (CPMT) Soc. IEEE; Electron. Components Assemblies & Mater. Assoc. (ECA); Electron. Components Sector of the Electron. Ind. Alliance
Conference Date: 29 May-1 June 2001 Conference Location: Orlando, FL, USA
Medium: Also available on CD-ROM in PDF format
Language: English Document Type: Conference Paper (PA)
Treatment: Experimental (X)
Abstract: Flip chip technology has been heavily focused on developing and refining the next generation of flip chip assembly and reliability; yet, little attention has been paid to the environmentally conscious aspects of manufacturing and high process throughput. Pending legislation restricting the use of lead in Europe and Japan and environmental concerns have forced flip chip technology to address new ways to meet safety and environmental requirements for the materials and processes used during assembly. The focus of this work is to implement advanced lead-free solder interconnect technology with halogen-free high density microvia substrates and define a systems-level low-cost flip chip material and process technology minimizing environmental impact. The ultimate objective is to ensure that environmentally friendly materials are selected, along with acceptable process technology for all materials as well as for the flip chip assembly. (7 Refs)
Subfile: B
Descriptors: environmental factors; flip-chip devices; soldering

16/7,DE/19 (Item 19 from file: 2)
DIALOG(R)File 2:INSPEC


7055106 INSPEC Abstract Number: B2001-11-0170J-129
Title: Wafer level interconnects with lead-free and low alpha solders
Author(s): Ning-Cheng Lee
Author Affiliation: Indium Corp. of America, Clinton, NY, USA
Conference Title: SMTA International Proceedings of the Technical Program p.826-35
Publisher: Surface Mount Technol. Assoc, Edina, MN, USA
Publication Date: 2000 Country of Publication: USA 952 pp.
Material Identity Number: XX-2000-01486
Conference Title: Proceedings of SMTA International
Conference Date: 24-28 Sept. 2000 Conference Location: Rosemont, IL, USA
Medium: Also available on CD-Rom in PDF format
Language: English Document Type: Conference Paper (PA)
Treatment: Practical (P); Experimental (X)
Abstract: Promising Pb-free solder alternatives for surface mount assembly include eutectic Sn/Ag, eutectic Sn/Cu, Sn95/Sb5, eutectic Sn/Bi, Sn/Ag/Cu, Sn/Ag/Cu/X, Sn/Bi/Ag/X, Sn/Zn/X, and Sn/In/Ag/(X). However, for wafer level area array solder bump interconnects, most of those options fall short in terms of fatigue resistance. Sn/In/Ag/(X) appears to be superior when compared with Sn63/Pb37, as demonstrated by Sn/In/Ag/Cu. For applications involving high Pb solders, no solder alternatives have been developed yet. While the industry is advancing toward finer, smaller, lighter, and faster, wafer level packages using area array solder interconnects are suffering from soft errors due to alpha particle emissions from Pb in the solders. Although Pb-free solder alternatives for eutectic Sn/Pb are virtually free from alpha emissions, the continuous dependence on the use of high-Pb solders for C4 applications indicates that the challenge of alpha emissions from Pb-containing solders will persist regardless of the Pb-free moves of the industry. This challenge is getting tougher with the rapid advancement of IC design toward further miniaturization. Low alpha lead can be obtained from cold lead ore, old lead, and the laser isotope separation process, with the latter having potential as a long term solution. Low alpha lead is very expensive when compared with regular lead. Due to the increase in I/O density, required alpha emission levels may soon move from LC2 to LC3 level. The supply of low alpha lead for wafer level interconnects does not seem to be an issue. (21 Refs)
Subfile: B
Descriptors: alpha-particle effects; ball grid arrays; chip scale packaging; environmental factors; fatigue; integrated circuit interconnections; integrated circuit reliability; laser isotope separation; microassembling; soldering


16/7,DE/20 (Item 20 from file: 2)
DIALOG(R)File 2:INSPEC


7048457 INSPEC Abstract Number: B2001-11-2210D-021
Title: Board level reliability of lead free soldered interconnections
Author(s): Albrecht, H.-J.
Author Affiliation: Siemens AG, Berlin, Germany
Conference Title: SMTA International Proceedings of the Technical Program

p.394-401
Publisher: Surface Mount Technol. Assoc, Edina, MN, USA
Publication Date: 2000 Country of Publication: USA 952 pp.
Material Identity Number: XX-2000-01486
Conference Title: Proceedings of SMTA International
Conference Date: 24-28 Sept. 2000 Conference Location: Rosemont, IL, USA
Medium: Also available on CD-Rom in PDF format
Language: English Document Type: Conference Paper (PA)
Treatment: Practical (P); Experimental (X)
Abstract: Recently, lead-free activities have taken center stage in the electronics package and assembly industry worldwide. Lead is widely reported to be related to certain health risks, and Japan, the USA and Europe have taken initiatives to reduce and eliminate lead in interconnection materials. In this paper, environmentally benign solders are discussed relative to their ability to interact with different surface finishes on packages and boards, for compatibility with existing process parameters and for board level reliability compared to conventional solder materials. The material selection is done based on the results of the European Ideals Project (Warwick, 1999) and further demands for successful lead-free solder implementation, e.g. low melting point, and high fatigue resistance for extended applications from an operating viewpoint. Including the Ideals activities to date, 211 lead-free alloys (pastes) were tested for wetting, spreading, dissolution, reflow profile optimization, 3D defects in comparison with organic vehicles used in the solder paste, interaction with conventional and lead-free finishes on packages and boards, intermetallic formation and fatigue properties. In order to characterize the primary alloy of choice, accelerated aging tests such as TCTs and PCTs were used to analyze board level reliability of various solder pastes. The paper outlines Pb-free paste analysis compared to conventional solder paste for conventional SMD components and CSPs. Important points of interest are processability relative to existing SMD processes and the board level reliability, which are primary acceptance criteria for implementation. (16 Refs)
Subfile: B
Descriptors: ageing; assembling; chip scale packaging; circuit reliability; dissolving; environmental factors; fatigue; health hazards; integrated circuit interconnections; melting point; optimisation; printed circuit manufacture; printed circuit testing; reflow soldering; surface mount technology; thermal stresses; wetting


16/7,DE/21 (Item 21 from file: 2)
DIALOG(R)File 2:INSPEC


7027140 INSPEC Abstract Number: B2001-10-0170J-020
Title: Pb-free solders for flip-chip interconnects
Author(s): Frear, D.R.; Jang, J.W.; Lin, J.K.; Zhang, C.
Author Affiliation: Interconnect Syst. Labs., Motorola Inc., Tempe, AZ, USA
Journal: JOM vol.53, no.6 p.28-32, 38
Publisher: Minerals, Metals & Mater. Soc,
Publication Date: June 2001 Country of Publication: USA
CODEN: JOMMER ISSN: 1047-4838
SICI: 1047-4838(200106)53:6L.28:FSFC;1-E
Material Identity Number: M963-2001-007
Language: English Document Type: Journal Paper (JP)
Treatment: Practical (P); Experimental (X)

Abstract: A variety of lead-free solder alloys were studied for use as flip-chip interconnects including Sn-3.5Ag, Sn-0.7Cu, Sn-3.8Ag-0.7Cu, and eutectic Sn-37Pb as a baseline. The reaction behaviour and reliability of these solders were determined in a flip-chip configuration using a variety of under-bump metallurgies (TiW-Cu, electrolytic nickel, and electroless Ni-P/Au). The solder microstructure and intermetallic reaction products and kinetics were determined. The Sn-0.7Cu solder has a large grain structure and the Sn-3.5Ag and Sn-3.8Ag-0.7Cu have a fine lamellar two-phase structure of tin and Ag/sub 3/Sn. The intermetallic compounds were similar for all the lead-free alloys. On Ni, Ni/sub 3/Sn/sub 4/ formed and on copper, two-phase Cu/sub 6/Sn/sub 5/Cu/sub 3/Sn formed. During reflow, the intermetallic growth rate was faster for the lead-free alloys, compared to eutectic tin-lead. In solid-state aging, however, the interfacial intermetallic compounds grew faster with the tin-lead solder than for the lead-free alloys. The reliability tests performed included shear strength and thermomechanical fatigue behaviour. The lower strength Sn-0.7Cu alloy also had the best thermomechanical fatigue behaviour. Failures occurred near the solder/intermetallic interface for all alloys except Sn-0.7Cu, which deformed by grain sliding and failed in the center of the joint. Based on this study, the optimal solder alloy for flip-chip applications is identified as eutectic Sn-0.7Cu. (33 Refs)

Subfile: B

Descriptors: ageing; circuit optimisation; crystal microstructure; fatigue; flip-chip devices; integrated circuit interconnections; integrated circuit packaging; integrated circuit reliability; interface structure; microassembling; reflow soldering; shear strength



16/7,DE/22 (Item 22 from file: 2)
DIALOG(R)File 2:INSPEC


7008705 INSPEC Abstract Number: A2001-18-6825-008

Title: Interfacial embrittlement by bismuth segregation in copper/tin-bismuth Pb-free solder interconnect

Author(s): Liu, P.L.; Shang, J.K.

Author Affiliation: Dept. of Mater. Sci. & Eng., Illinois Univ., Urbana, IL, USA

Journal: Journal of Materials Research vol.16, no.6 p.1651-9

Publisher: Mater. Res. Soc,

Publication Date: June 2001 Country of Publication: USA

CODEN: JMREEE ISSN: 0884-2914

SICI: 0884-2914(200106)16:6L.1651:IEBS;1-8

Material Identity Number: I870-2001-006

U.S. Copyright Clearance Center Code: 0884-2914/2001/$2.50

Language: English Document Type: Journal Paper (JP)

Treatment: Experimental (X)

Abstract: Microchemistry and mechanical properties of a copper/tin-bismuth Pb-free solder interconnect were examined in the as-reflowed and aged conditions by in situ Auger fracture and interface fracture mechanics techniques. In the as-reflowed condition, the solder-copper interface was highly resistant to fracture, and the fracture mechanism was ductile with the crack path following the interface between the solder alloy and the copper-tin intermetallic phase. Upon thermal aging, bismuth segregation was found to occur on the copper-intermetallic interface. Auger depth profiling indicated that the segregation was confined to about one monolayer from the interface. The segregation was shown to embrittle the interface, resulting in an approximately 5-fold decrease in the interfacial fracture resistance. (32 Refs)

Subfile: A
Descriptors: ageing; bismuth alloys; chemical interdiffusion; copper; ductile fracture; embrittlement; fracture mechanics; metallisation; reflow soldering; surface segregation; tin alloys


16/7,DE/27 (Item 27 from file: 2)
DIALOG(R)File 2:INSPEC


6715231 INSPEC Abstract Number: B2000-11-2210D-009
Title: Lead free soldering electronic interconnect: Current status and future developments
Author(s): Snowdon, K.G.; Tanner, C.G.; Thompson, J.R.
Author Affiliation: Nortel Networks, Harlow, UK
Conference Title: 2000 Proceedings. 50th Electronic Components and Technology Conference (Cat. No.00CH37070) p.1416-19
Publisher: IEEE, Piscataway, NJ, USA
Publication Date: 2000 Country of Publication: USA xxxv+1756 pp.
ISBN: 0 7803 5908 9 Material Identity Number: XX-2000-01366
U.S. Copyright Clearance Center Code: 0 7803 5908 9/2000/$10.00
Conference Title: 2000 Proceedings. 50th Electronic Components and Technology Conference
Conference Sponsor: Components, Packaging, and Manuf. Technol. Soc. of IEEE; Electronic Ind. Alliance
Conference Date: 21-24 May 2000 Conference Location: Las Vegas, NV, USA
Language: English Document Type: Conference Paper (PA)
Treatment: Experimental (X)
Abstract: There is world-wide concern about the potential ecological impacts of lead-based solders, present in old electronic equipment buried in landfill sites. This paper reports the results of over nine years R and D at Nortel Networks on identification, evaluation and deployment of lead-free solders for printed circuit board assembly. This work has resulted in the production of the world's first virtually lead-free telephone-the Nortel Meridian 8009-by using a lead-free, tin-copper solder. To date, this telephone has passed a battery of functional tests and logged over 3.5 years of fault-free operation in normal usage. Other applications include mobile telephones and backplanes for PABXs. The technical and economic criteria used to select the tin-copper alloy are described, together with progress in producing compatible HASL tin-copper PCB finishes and tin-copper plated finishes on components. Reliability aspects of this alloy are also discussed. The challenges remaining to implement this lead-free technology into more complex telecommunications components including array packages and chip scale semiconductors via the jetting of lead free alloy spheres are discussed. The replacement of high lead, high melting point circa. 280 degrees C solder alloys is another topic that will be addressed. (7 Refs)
Subfile: B
Descriptors: environmental factors; printed circuit manufacture; soldering


16/7,DE/34 (Item 34 from file: 2)
DIALOG(R)File 2:INSPEC


6238996 INSPEC Abstract Number: B1999-06-2210D-019

Title: Tin-silver-copper: a lead free solder for capacitor interconnects
Author(s): Anderson, I.E.
Author Affiliation: Ames Lab., Iowa State Univ., Ames, IA, USA
Conference Title: 16th Capacitor and Resistor Technology Symposium. CARTS '96 p.63-7
Publisher: Components Technol. Inst, Huntsville, AL, USA
Publication Date: 1996 Country of Publication: USA 320 pp.
Material Identity Number: XX-1996-00209
Conference Title: Proceedings of 16th Capacitor and Resistor Technology Symposium
Conference Sponsor: Components Technol. Inst.; IEEE; Microelecton. Soc
Conference Date: 11-15 March 1996 Conference Location: New Orleans, LA, USA
Language: English Document Type: Conference Paper (PA)
Treatment: Applications (A); New Developments (N); Practical (P); Experimental (X)
Abstract: A new family of Pb-free solder alloys based on Sn-Ag-Cu is being developed for use by the electronics industry in response to health and environmental concerns and to meet emerging requirements for solders with improved strength at ambient and elevated temperatures. The recent discovery of the ternary eutectic composition Sn-4.7 Ag-1.7 Cu (wt.%), with T/sub e/=217 degrees C, is the basis for the new solders, which can compete with Sn-Pb solders and Sn-Ag eutectic solder. Sn-Ag-Cu solder appears well suited for use in electronic packaging applications for harsh environments, e.g. automotive and avionics, but may also be applied broadly in electronics, capacitor interconnects, electrical and mechanical connectors, and heat exchanger manufacturing. This paper summarizes the initial discovery, phase diagram studies, and related microstructural analysis of the new ternary eutectic alloy. A brief description of applied studies with solder paste, wire, and bath processing results is also included. (6 Refs)
Subfile: B
Descriptors: assembling; capacitors; copper compounds; environmental factors; eutectic alloys; health hazards; interconnections; packaging; printed circuit manufacture; silver alloys; soldering; tin alloys


16/7,DE/37 (Item 37 from file: 2)
DIALOG(R)File 2:INSPEC


5242269 INSPEC Abstract Number: B9605-0170Q-009
Title: Lead free interconnect materials for the electronics industry
Author(s): Napp, D.
Author Affiliation: Nat. Center for Manuf. Sci., Ann Arbor, MI, USA
Conference Title: 27th International SAMPE Technical Conference. Diversity into the Next Century Vol.27 p.340-51
Editor(s): Martinez, R.J.; Arris, H.; Emerson, J.A.; Pike, G.
Publisher: Soc. Adv. Mater. & Process Eng, Covina, CA, USA
Publication Date: 1995 Country of Publication: USA xxi+1191 pp.
ISBN: 0 938994 73 5 Material Identity Number: XX96-00091
Conference Title: Proceedings of 27th SAMPE International Technical Conference
Conference Date: 9-12 Oct. 1995 Conference Location: Albuquerque, NM, USA
Language: English Document Type: Conference Paper (PA)
Treatment: General, Review (G); Practical (P)
Abstract: Considerable development and research has been conducted over the last 25 years by many areas of manufacturing to reduce the use of lead and to limit human exposure to lead and products containing lead. The

elimination of lead from all manufacturing products, whether through legislation or through tax incentives, will have a significant impact on electronic interconnect technologies. The National Center for Manufacturing Sciences (NCMS), a cooperative research consortium of more than 215 US North American manufacturers, established multi-year programs, Lead Free Solder Project (LFSP) and Conductive Polymer Interconnect Project (CPIP), involving participants from industry, academia, and national laboratories. The objective of these programs is to identify lead free solder alternative replacement(s) and conductive polymeric materials for lead bearing solders in the electronics industry. The new materials must meet the interconnect performance requirements at operating environments ranging from -55 to +180 degrees centigrade. Numerous lead free alloy solders, each exhibiting unique properties, have been used by electronic manufacturers in specific applications. The major usage of conductive adhesives has been in consumer electronics and children's toys. Before any of these new lead free materials can be applied to the widely diverse electronics industry, considerable research and development is required. The NCMS programs involve a study of the material properties, manufacturability, modeling and reliability predictions, economic impact, and toxicological properties. (0 Refs)

Subfile: B

Descriptors: adhesion; conducting polymers; electronics industry; environmental factors; health hazards; integrated circuit interconnections; soldering



16/7,DE/39 (Item 39 from file: 2)
DIALOG(R)File 2:INSPEC


4705895 INSPEC Abstract Number: B9408-2210D-016

Title: Alternatives of lead bearing solder alloys

Author(s): Melton, C.

Author Affiliation: Motorola, Schaumburg, IL, USA

p.94-7

Publisher: IEEE, New York, NY, USA

Publication Date: 1993 Country of Publication: USA viii+207 pp.

ISBN: 0 7803 0829 8

U.S. Copyright Clearance Center Code: 0 7803 0829 8/93/$03.00

Conference Title: Proceedings of 1993 IEEE International Symposium on Electronics and the Environment

Conference Sponsor: IEEE

Conference Date: 10-12 May 1993 Conference Location: Arlington, VA, USA

Language: English Document Type: Conference Paper (PA)

Treatment: Practical (P)

Abstract: Proposed legislation and regulation dealing with the use of lead in commercial products are the main driving forces in the search for lead-free solder replacements in printed circuit board assembly. Research into potential replacements for the use of lead-tin solder in surface mount applications has prompted examination of alternative interconnect materials which not only include lead-free solder alloys but also address the use of nonmetallic-based attachment systems. The author discusses the available free-lead substitutes with emphasis on performance considerations and current processing changes that might be warranted due to the use of alternative interconnected materials. The choice of a joining material will necessitate consideration and optimization of the entire assembly process, its individual constituents, and the resulting performance. A significant development effort will be required for joining material substitution to

present assembly practices and successful implementation into electronic product manufacturing. (5 Refs)
Subfile: B
Descriptors: assembling; legislation; printed circuit manufacture; soldering; surface mount technology

16/7,DE/40 (Item 1 from file: 347)
DIALOG(R)File 347:JAPIO


01313681
COOLED TYPE PHOTOELECTRIC CONVERSION DEVICE

PUB. NO.: 59-025281 [JP 59025281 A]
PUBLISHED: February 09, 1984 (19840209)
INVENTOR(s): ROKUSHIYA KIYOSHI
APPLICANT(s): FUJITSU LTD [000522] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 57-134135 [JP 82134135]
FILED: July 30, 1982 (19820730)
JAPIO CLASS: 42.2 (ELECTRONICS -- Solid State Components)
JAPIO KEYWORD:R022 (ULTRALOW TEMPERATURES)

ABSTRACT

PURPOSE: To stably solder adjacent lead wirings without being interconnected by reforming the structure of solder for connection between the lead wirings and lead conductors.

CONSTITUTION: A heat insulating vessel of Dewar structure consists of an outer cylinder 1 provided with a photo transmission window 3 and an inner cylinder 2 arranged with a photoelectric conversion element 5 on a cooling base 4. A plurality of lead wiring films 7 are arranged on the outer peripheral surface of the inner cylinder 2, and a solder film 12 of an AuGe alloy, etc. is adhesion- formed at the end parts 7a and 7b. Conductive film patterns 9 which lead signal out of the tube are provided on a ceramic terminal material 8 sealed in the form of transverse across a part of the vessel wall of the outer cylinder 1. The lead conductors 10 and 11 of lead frame constitution fixed previously to the photoelectric conversion element 5 and the conductive film patterns 9 are thermally fixed by pressure and connected respectively to each connection end part 7a and 7b of the lead wiring films 7 via the solder film 12.

16/7,DE/43 (Item 3 from file: 350)
DIALOG(R)File 350:Derwent WPIX


015140177
WPI Acc No: 2003-200704/200319
Solder interconnect structure for electronic package, has joiner interconnect with lead-free joiner solder whose liquidus temperature is less than solidus temperature of lead-free core solder of core interconnect
Patent Assignee: SARKHEL A K (SARK-I); INT BUSINESS MACHINES CORP (IBMC )
Inventor: SARKHEL A K
Number of Countries: 001 Number of Patents: 002
Patent Family:

| Patent No | Kind | Date | Applicat No | Kind | Date | Week |
|---|---|---|---|---|---|---|
| US 20020192443 | A1 | 20021219 | US 2000660558 | A | 20000912 | 200319 B |

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| | | | US 2002197291 | A | 20020716 | | |
| US 6581821 | B2 | 20030624 | US 2000660558 | A | 20000912 | 200343 | |
| | | | US 2002197291 | A | 20020716 | | |

Priority Applications (No Type Date): US 2000660558 A 20000912; US 2002197291 A 20020716
Patent Details:

| Patent No | Kind | Lan | Pg | Main IPC | Filing Notes |
|---|---|---|---|---|---|
| US 20020192443 | A1 | | 10 | B32B-003/00 | Div ex application US 2000660558<br>Div ex patent US 6433425 |
| US 6581821 | B2 | | | B23K-031/02 | Div ex application US 2000660558<br>Div ex patent US 6433425 |

Abstract (Basic): US 20020192443 A1
Abstract (Basic):

NOVELTY - The solder structure (15) has a joiner interconnect (18,34) provided with a lead-free joiner solder and has a core interconnect (46) provided with a lead-free core solder. The joiner interconnect solderably couples one end of core interconnect to the electronic component (12,30).

A liquidus temperature of joiner solder is less than the solidus temperature of core solder.

DETAILED DESCRIPTION - An INDEPENDENT CLAIM is included for method of forming electronic structure.

USE - Used for electronic package to couple a chip carrier to circuit card.

ADVANTAGE - Provides a lead-free solder interconnect structure for coupling a chip carrier to a circuit card.

DESCRIPTION OF DRAWING(S) - The figure shows the front, cross-sectional view of the solder interconnect structure.

electronic component (12,30)
solder structure (15)
joiner interconnect (18,34)
core interconnect (46)
pp; 10 DwgNo 1/2

Title Terms: SOLDER; INTERCONNECT; STRUCTURE; ELECTRONIC; PACKAGE; JOINER; INTERCONNECT; LEAD; FREE; JOINER; SOLDER; LIQUIDUS; TEMPERATURE; LESS; SOLIDUS; TEMPERATURE; LEAD; FREE; CORE; SOLDER; CORE; INTERCONNECT
Derwent Class: L03; P55; P73; U11; V04
International Patent Class (Main): B23K-031/02; B32B-003/00
International Patent Class (Additional): H01L-023/48

16/7,DE/44 (Item 4 from file: 350)
DIALOG(R)File 350:Derwent WPIX


014928477
WPI Acc No: 2002-749186/200281
Electronic structure, for use in forming electronic package, includes interconnect structures comprising joiner solder and core solder that are lead free
Patent Assignee: INT BUSINESS MACHINES CORP (IBMC )
Inventor: SARKHEL A K
Number of Countries: 001 Number of Patents: 001
Patent Family:

| Patent No | Kind | Date | Applicat No | Kind | Date | Week | |
|---|---|---|---|---|---|---|---|
| US 6433425 | B1 | 20020813 | US 2000660558 | A | 20000912 | 200281 | B |

Priority Applications (No Type Date): US 2000660558 A 20000912

Patent Details:
Patent No  Kind Lan Pg   Main IPC    Filing Notes
US 6433425    B1     8 H01L-023/48

Abstract (Basic): US 6433425 B1
Abstract (Basic):
NOVELTY - An electronic structure comprises electronic component and solder structure. The solder structure has joiner interconnect having joiner solder and core interconnect having core solder. The joiner and core solder are lead free. The joiner couples core interconnect end to electronic component. A liquidus temperature of joiner solder is less than a solidus temperature of the core solder.
USE - Forming electronic package.
ADVANTAGE - The structure does not comprise any lead component that is toxic and environmentally hazardous.
DESCRIPTION OF DRAWING(S) - The drawing shows a front, cross-section of an electronic structure including core interconnect of solder ball.
Electronic components (12, 30)
Core interconnect (16)
Joiner solder (18)
pp; 8 DwgNo 2/2
Title Terms: ELECTRONIC; STRUCTURE; FORMING; ELECTRONIC; PACKAGE; INTERCONNECT; STRUCTURE; COMPRISE; JOINER; SOLDER; CORE; SOLDER; LEAD; FREE
Derwent Class: L03; M23; M26; U11; V04; X24
International Patent Class (Main): H01L-023/48

16/7,DE/45     (Item 5 from file: 350)
DIALOG(R)File 350:Derwent WPIX


014650905
WPI Acc No: 2002-471609/200250
Lead-free solder alloy for use in solder interconnections in microelectronics and electronic applications has preset liquidus melting temperature and includes tin, copper, silver and indium
Patent Assignee: H TECHNOLOGIES GROUP INC (HTEC-N); MEDDLE A L (MEDD-I); SINGAPORE ASAHI CHEM & SOLDER IND PTE LT (ASAH )
Inventor: MEDDLE A L; GUO Z; HWANG J S
Number of Countries: 090  Number of Patents: 003
Patent Family:

| Patent No | Kind | Date | Applicat No | Kind | Date | Week | |
|---|---|---|---|---|---|---|---|
| WO 200240213 | A1 | 20020523 | WO 2000GB4365 | A | 20001116 | 200250 | B |
| AU 200114037 | A | 20020527 | WO 2000GB4365 | A | 20001116 | 200261 | |
| | | | AU 200114037 | A | 20001116 | | |
| NO 200302185 | A | 20030514 | WO 2000GB4365 | A | 20001116 | 200354 | |
| | | | NO 20032185 | A | 20030514 | | |

Priority Applications (No Type Date): WO 2000GB4365 A 20001116
Patent Details:
Patent No  Kind Lan Pg   Main IPC    Filing Notes
WO 200240213  A1 E  20 B23K-035/26
Designated States (National): AE AL AM AT AU AZ BA BB BG BR BY CA CH CN CR CU CZ DE DK DM EE ES FI GB GD GE GH GM HR HU ID IL IN IS JP KE KG KP KR KZ LC LK LR LS LT LU LV MA MD MG MK MN MW MX NO NZ PL PT RO RU SD SE SG SI SK SL TJ TM TR TT TZ UA UG UZ VN YU ZA ZW
Designated States (Regional): AT BE CH CY DE DK EA ES FI FR GB GH GM GR IE IT KE LS LU MC MW MZ NL OA PT SD SE SL SZ TR TZ UG ZW

AU 200114037 A B23K-035/26 Based on patent WO 200240213
NO 200302185 A B23K-035/26

Abstract (Basic): WO 200240213 A1
Abstract (Basic):
NOVELTY - Lead-free solder alloy has liquidus melting temperature below 215 degrees C and consists essentially of 76-96% of tin (Sn), 0.2-2.5% of copper (Cu), 2.5-4.5% of silver (Ag) and above 0 to 12% (preferably up to 8%) of indium (In).
DETAILED DESCRIPTION - INDEPENDENT CLAIMS are given for lead free solder alloys containing:
(i) 76-96% Sn, 0.2-2.5% Cu, 2.5-4.5% Ag, above 0 to 12% In and above 0 to 2% antimony,
(ii) 76-96% Sn, 0.2-2.5% Cu, 2.5-4.5% Ag, above 0 to 12% In and 0.5-5% bismuth (Bi) and having liquidus melting temperature below about 215 degrees C,
(iii) 76-96% Sn, 0.2-2.5% Cu, 2.5-4.5% Ag, above 0 to 12% In, 0.5-5% Bi and above 0 to 2% antimony (Sb), or
(g) 76-96% Sn, 0.2-2.5% Cu, 2-3.5% Ag, 0.5-5% bismuth.
USE - For use in soldering and solder interconnections, in microelectronics and electronics applications.
ADVANTAGE - The lead free solder has high-strength, and high fatigue resistance to withstand the increasingly adverse and harsh conditions in microelectronic and electronic applications. Lead-free solder has a moderate melting range. Lead-free solder alloy can readily wet common metallic substrates such as Sn, Cu, Ag, Au, Pd and Ni in microelectronic and electronic manufacturing to form sound and reliable solder joints without fluxes that are unacceptable to electronic manufacturing. Lead-free solder can adapt to the established electronic manufacturing process and infrastructure without requiring major changes in materials, processes and components. The alloy can be used as paste, powder, bars and wires or in soldering processes such as reflow oven soldering, wave machine and hand soldering, in materials fabrication such as various deposition and coating techniques.
DESCRIPTION OF DRAWING(S) - The figure shows the wetting force (mN) vs. wetting time of the solder alloy: 82.3%Sn-0.5%Cu-3%Ag-2.2%Bi-12%In on a Cu coupon at 235 degrees C.
pp; 20 DwgNo 1/1
Title Terms: LEAD; FREE; SOLDER; ALLOY; SOLDER; INTERCONNECT; MICROELECTRONIC; ELECTRONIC; APPLY; PRESET; LIQUIDUS; MELT; TEMPERATURE; TIN; COPPER; SILVER; INDIUM
Derwent Class: L03; M23; M26; P55; V04
International Patent Class (Main): B23K-035/26
International Patent Class (Additional): C22C-013/00

16/7,DE/46 (Item 6 from file: 350)
DIALOG(R)File 350:Derwent WPIX


013617877
WPI Acc No: 2001-102085/200111
Lead-free solder alloy for soldering interconnections in microelectronics and electronics applications comprises tin, copper, silver, and indium
Patent Assignee: HIGH SCI & TECHNOLOGY GROUP CO (HIGH-N); H TECHNOLOGIES GROUP INC (HTEC-N)
Inventor: GUO Z; HWANG J S
Number of Countries: 002 Number of Patents: 002
Patent Family:
Patent No Kind Date Applicat No Kind Date Week

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| US 6176947 | B1 | 20010123 | US 98224323 | A | 19981231 | 200111 | B |
| | | | US 99417169 | A | 19991012 | | |
| CN 1314229 | A | 20010926 | CN 2000135326 | A | 20001012 | 200206 | |

Priority Applications (No Type Date): US 98224323 A 19981231; US 99417169 A 19991012

Patent Details:

| Patent No | Kind | Lan | Pg | Main IPC | Filing Notes |
|---|---|---|---|---|---|
| US 6176947 | B1 | | 6 | C22C-007/00 | Cont of application US 98224323 |
| CN 1314229 | A | | | B23K-035/26 | |

Abstract (Basic): US 6176947 B1

Abstract (Basic):

NOVELTY - A lead-free solder alloy comprises 76-96 wt. % tin, 0.2-2.5 wt.% copper, 2.5-4.5 wt.% silver, and 6-12 wt.% indium having a liquidus melting temperature below 215degreesC.

USE - For soldering interconnections in microelectronics and electronics applications, e.g., mainstream electronics manufacturing.

ADVANTAGE - The inventive alloy provides high strength, high fatigue resistance and high wetting ability having the compatible melting temperature with the established printed circuit board manufacturing infrastructure. It forms reliable joints.

pp; 6 DwgNo 0/1

Title Terms: LEAD; FREE; SOLDER; ALLOY; SOLDER; INTERCONNECT; MICROELECTRONIC; ELECTRONIC; APPLY; COMPRISE; TIN; COPPER; SILVER; INDIUM

Derwent Class: M26; P55; U11; X24

International Patent Class (Main): B23K-035/26; C22C-007/00